Fast input-voltage transient response with digitally-controlled isolated DC/DC converters

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Introduction

Telecommunications equipment is often subjected to environmental and other electrical stresses such as lightning strikes, equipment faults, and capacitor-bank switching. These events can cause input-voltage transients of up to 100 V for durations of 10 ms. Various telecommunications standards, including the American National Standard (ANSI T1.315-2001 Specification) and Alliance for Telecommunications Industry Solutions (ATIS-0600315.2007 Specification), dictate the behavior of DC-powered equipment used in telecommunications environments.

In particular, these standards stipulate required behaviors when exposed to overvoltage transients. Overvoltage-transient conformance to the above specifications requires that a power supply must:

- Be able to handle an input surge voltage of 100 V for 10 ms
- Not be damaged or result in performance degradation

The design goals for today's state-of-the-art isolated DC/DC converters generally target an output voltage disturbance of less than 10% for all transient conditions of the input voltage. A large overshoot at the output may damage the downstream equipment and a big output-voltage undershoot can cause the equipment to shut down or reset. In the case of isolated DC/DC converters with synchronous rectification, a large reverse current may be generated that subjects electrical components to overstress and increases system noise, thus, disturbing the converter's normal operation.

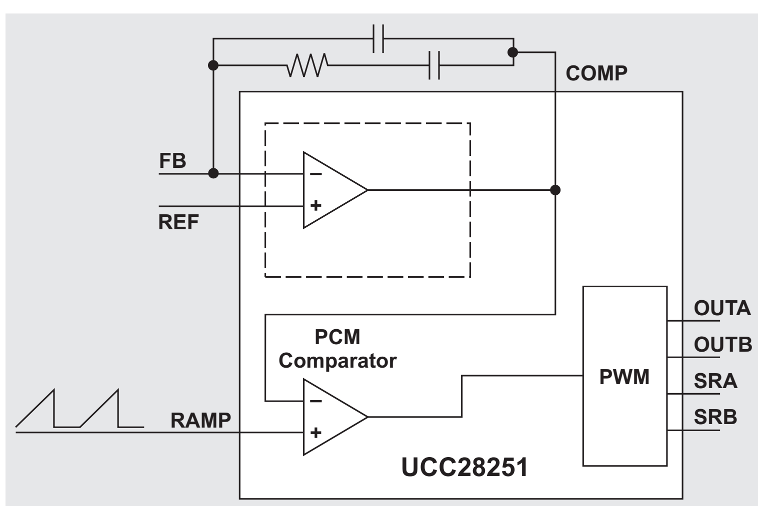
One condition that a designer must be mindful of is the input-voltage slew rate. An extremely-fast voltage slew rate (for example, 50 V to 75 V in 2 µs) often can cause the output-voltage disturbance to exceed ±10%. It is unlikely that these standards will be relaxed any time soon. In fact, these conditions most likely will become even more stringent. Therefore, today's isolated DC/DC power supplies must have a very good control method (or voltage feed forward) to limit the magnitude of the output-voltage undershoot and overshoot caused by an input-voltage transient.

Input-voltage feed forward within the power supply's nominal input range

A huge challenge for designers of digitally-controlled isolated DC/DC converters is the attenuation of the output-voltage fluctuations during abrupt input-voltage transients that are within the power supply's nominal input voltage range. However, in traditional primary-side controlled solutions (Figure 1), this is easy to manage. The sawtooth signal to the comparator has a peak value that is proportional to the input voltage and is used to terminate the duty cycle of the pulse-width modulator (PWM). In this way, the product of the input voltage and primary turn-on time is almost a constant value, no matter how fast the input voltage changes. Using this method, the output voltage has a very fast response for line-input transients.

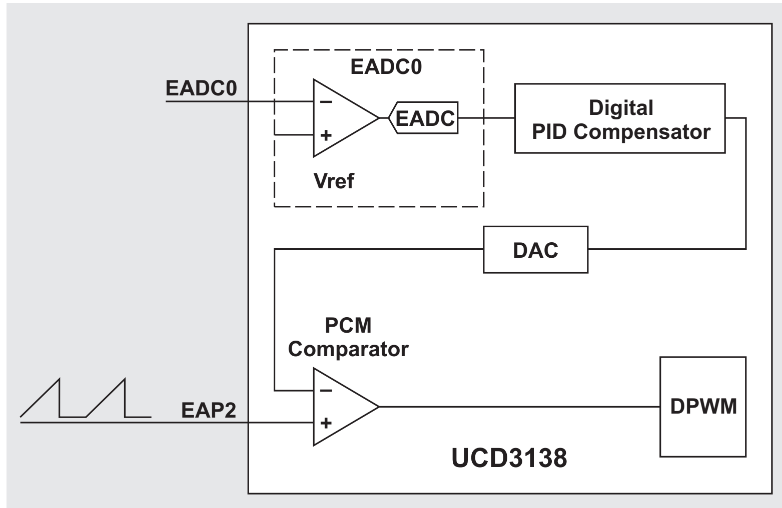
In digitally-controlled solutions, the digital controller is usually located on the transformer's secondary or output side. This allows the controller to achieve a better load-transient response and to easily perform communication with the host microcontroller via I^2C or PMBus™.

Figure 1. Analog controller with PWM generation



Compared with a primary analog controller solution, it becomes more difficult for the digital controller to quickly and accurately detect the input voltage transients occurring on the transformer's primary side. In a purely digital solution, the designer must consider further complexities such as A/D conversion delay, digital processing delay, and digital pulse-width modulator (DPWM) generating delay.

Figure 2. A digital controller configured similar to an analog PWM controller



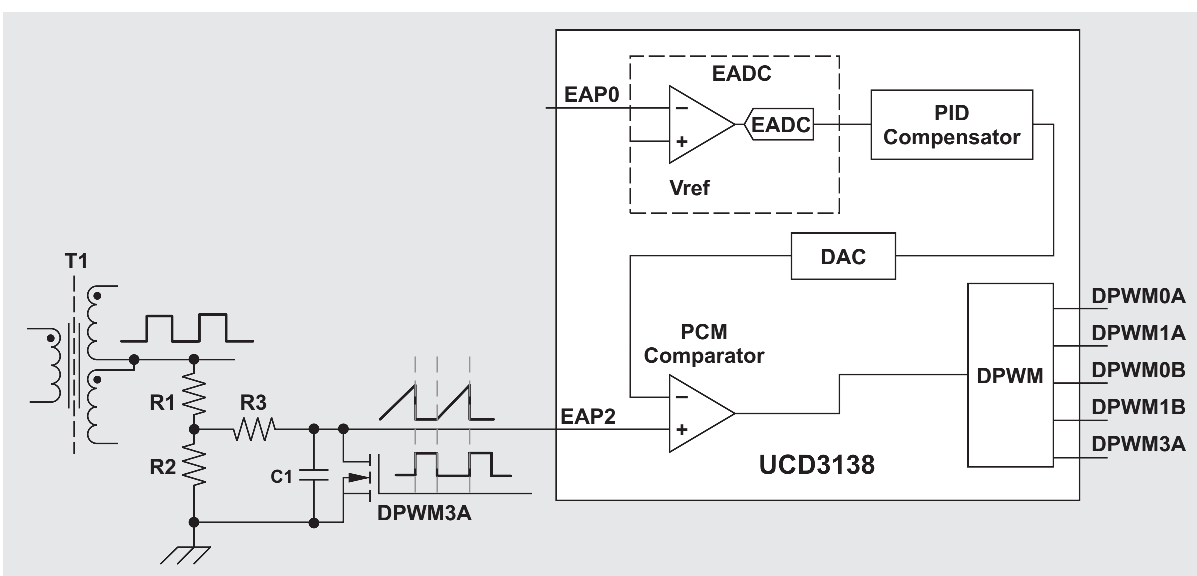
Solution

It is possible for a digitally-controlled solution to control duty cycle much like the analog solution. This means that the digital-power controller in Figure 2 can be configured with similar performance to the analog controller in Figure 1 while maintaining its digital flexibility.

The key challenge is how to generate a ramp similar to the analog solution. In buck-derived DC/DC isolated topologies, input voltage can be reflected on the transformer's secondary winding during the effective on time of the primary switch. The hard-switching full-bridge (HSFB) topology shown in Figure 3 is an example of the method for generating this ramp.

T1 represents the power transformer used in the HSFB topology. When a pair of primary switches are turned on, the input voltage reflected on the secondary winding charges C1 through R1 and R3. This continues until the PCM comparator terminates the pulse of the primary gate driver when the sawtooth voltage on the EAP2 pin exceeds the DAC's output. DPWM3A is a complementary signal of the primary gate driver that is generated by the digital controller. This controller is used to discharge C1 at every half switching cycle. R2 is added to limit the voltage on the EAP2 pin, which is lower than its maximum voltage rating at any condition.

Figure 3. RAMP generation with HSFB topology



Test results

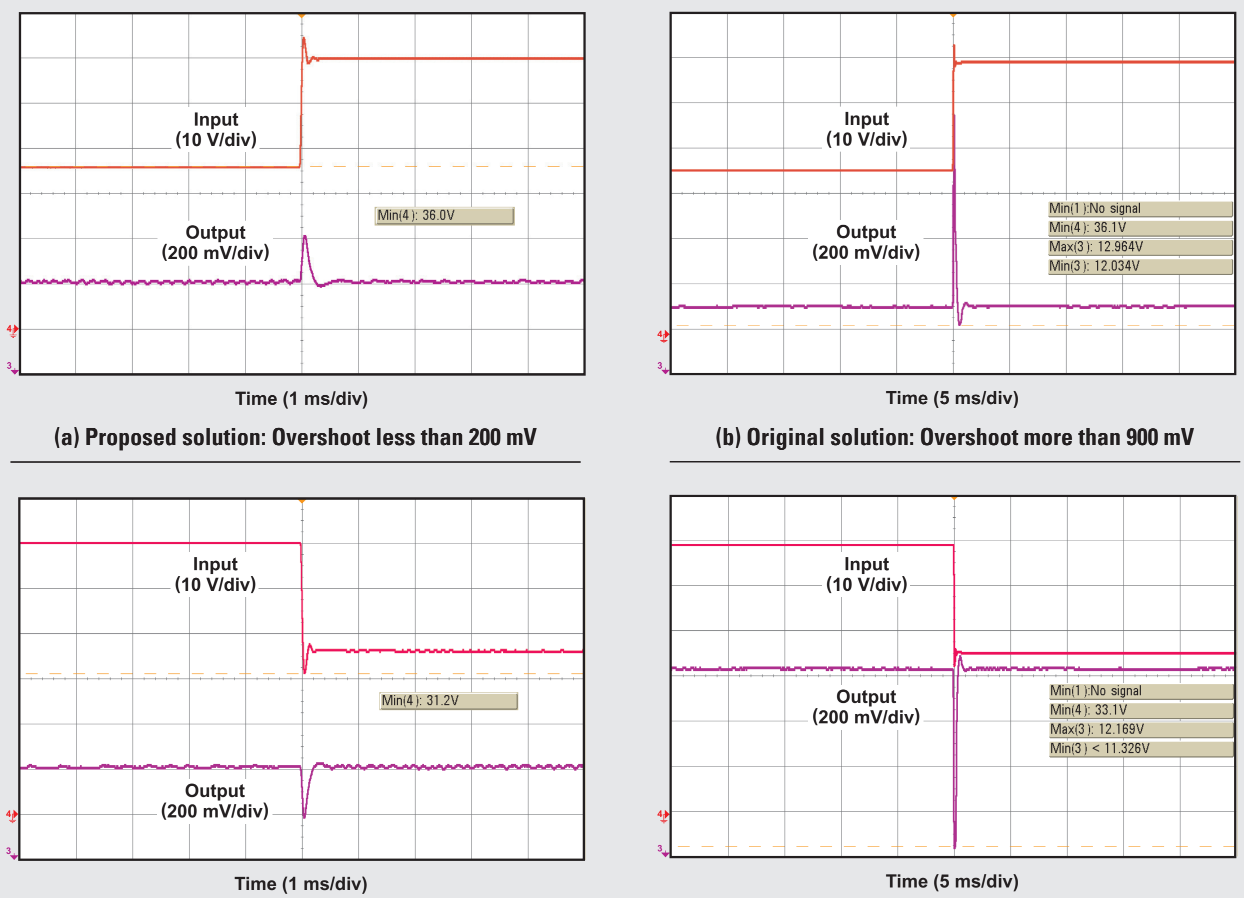
The test comparison in Figure 4 was generated with the UCD3138HSFBEVM-029 evaluation module (EVM), which is a HSFB demo module with a 12-V output. This EVM employs a non-linear multiplier solution to implement input-voltage feed-foward control that can achieve a good output response. However, the method proposed here can achieve an even better performance. The amplitude of both overshoot and undershoot is reduced by four times when the input voltage steps between 36 V and 60 V with a voltage slew rate of 1 V/µs. The 36-V minimum voltage of this transience test was chosen because the output voltage cannot maintain below that limit, or output voltage-hold threshold.

Avoid reverse current when input voltage drops below the output voltage-hold threshold

When the input voltage drops below the output voltage-hold threshold, the duty cycle reaches its maximum value. Now the product of the input voltage and duty cycle decreases. If the power stage still operates in the synchronous rectification mode, this causes the energy stored in the output capacitor to flow in a reverse direction to the input.

The reverse current could be huge, which may cause overcurrent stress on the power train. A popular solution is to add a reverse-current protection circuit where the synchronous rectifier (SR) is turned off when reverse

Figure 4. A comparison test for input-voltage transients between 36 V and 60 V



(a) Proposed solution: Overshoot less than 200 mV

(b) Original solution: Overshoot more than 900 mV

(c) Proposed solution: Undershoot less than 200 mV

(d) Original solution: Undershoot more than 800 mV current is larger than a safe threshold. This way, the loop of the reverse current through the output inductance is cut off abruptly. The energy stored in the output inductance, causes an avalanche breakdown of the SR, which can cause SR failure.

Solution

To solve this problem, a voltage-detection circuit can turn off the SR immediately. This occurs before the reverse current is generated and when the input voltage drops to lower than the output voltage-hold threshold. The circuit shown in Figure 5 detects the input voltage from the transformer's center tap (V_TAP). The EAP1 pin, which belongs to the UCD3138 front-end block, can be configured to sample the voltage only at the on-time of the primary switch when the V-TAP's voltage reflects an input voltage.

In Figure 6, the scaled down input voltage is converted to a digital number stored in the ABS registers. A pair of digital window comparators inside the digital controller are configured to detect the undervoltage input and the input-voltage recovery. When an input voltage below the output voltage-hold threshold is detected, within nanoseconds, digital comparator 0 issues a fault signal to the DWPM module to shut down the DMPM0B/1B, SR-gate drive signal. When the input voltage recovers, the digital comparator 1 triggers a fast firmware interruption that enables the SR-gate driver. A pre-bias startup routine is started so that the output voltage can recover in the shortest amount of time.

Figure 5. Input-voltage detection circuit

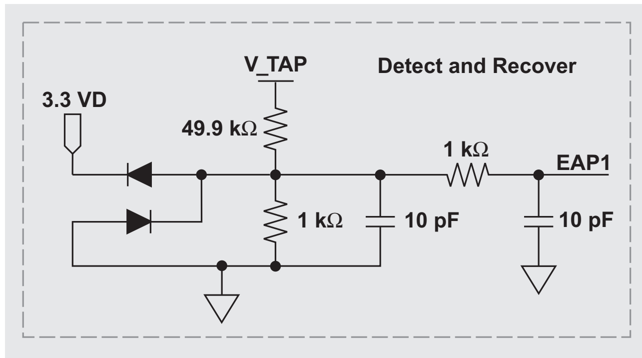


Figure 6. Turn-on/off control of a synchronous rectifier

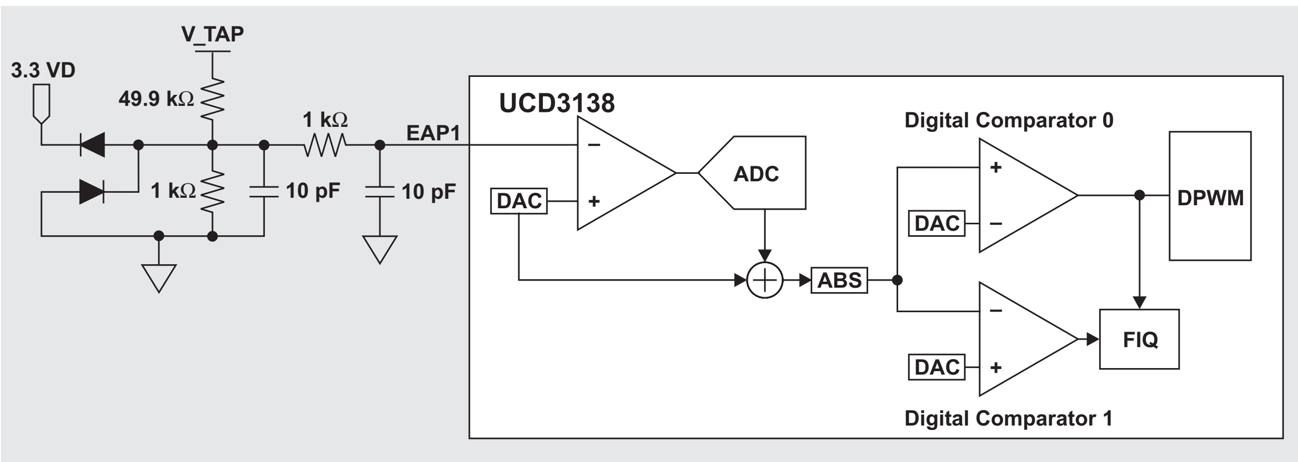
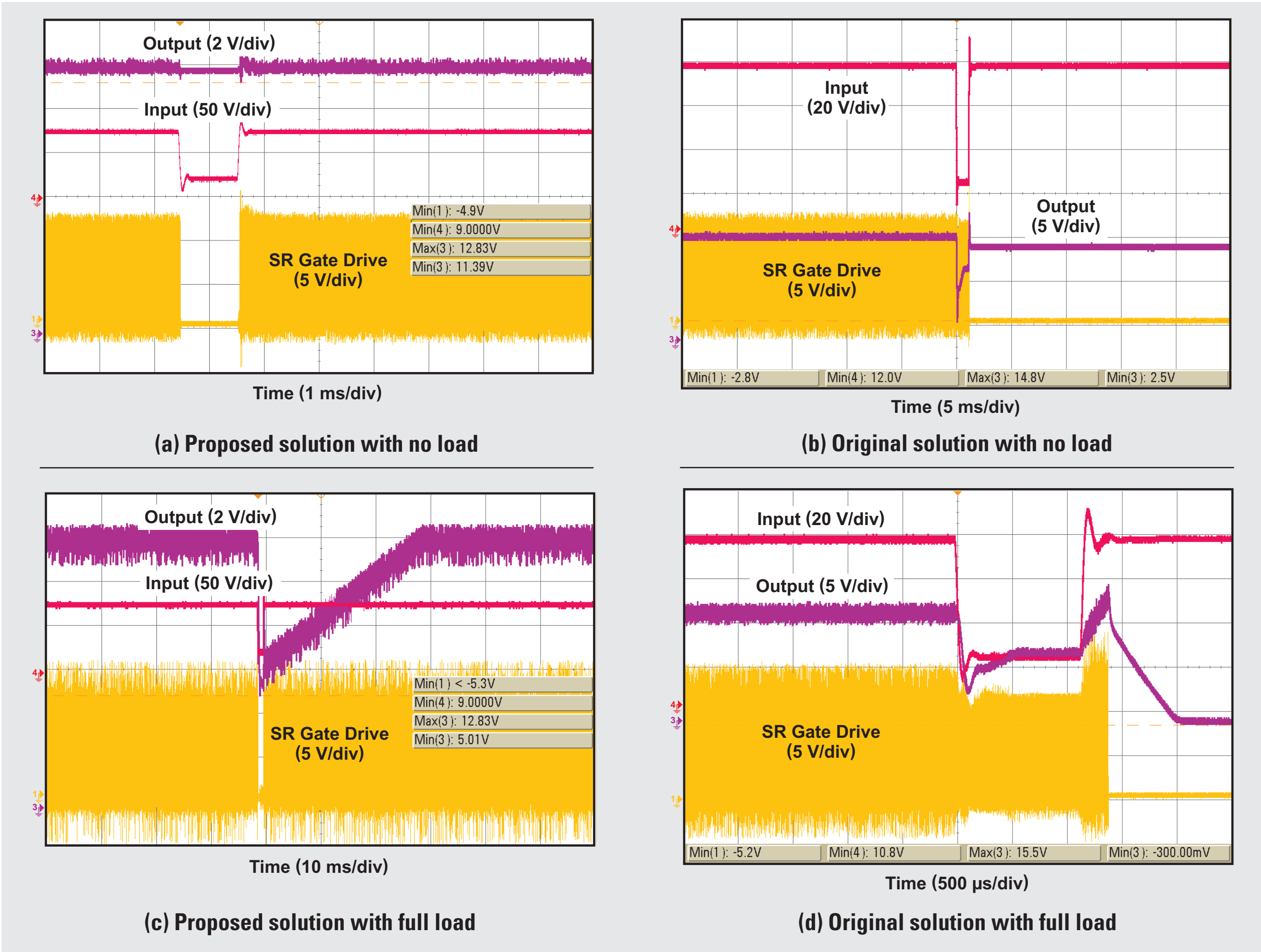


Figure 7. Test results when the input-voltage transient is between 60 V and 20 V



(a) Proposed solution with no load
(b) Original solution with no load
(c) Proposed solution with full load
(d) Original solution with full load

Test results

The proposed solution is designed to shut down the SR gate driver signal as soon as the input voltage drops below 36 V (Figure 7a). There is no reverse current discharging the output capacitor and the output voltage under no-load test barely changes while the input voltage stays at 22 V. In comparison, the original SR gate-driver EVM solution (Figure 7b) continues to run, even though the input voltage is below 36 V. The reverse current is generated, causing the output voltage to be discharged, even under no-load conditions.

The original EVM solution does not have a pre-bias start-up function when the input voltage recovers to its normal value, which causes an output voltage overshoot and triggers OVP after the input voltage recovers (Figure 7d). For a full-load test, the output voltage in the proposed solution is discharged by the load (Figure 7c). When the input voltage recovers, the output can immediately and monotonously rise back to the regulated voltage, which is controlled by the pre-bias startup routine.

Conclusion

It was shown that a secondary-side, digitally-controlled solution provides good performance under line-transient test conditions.

A proposed solution showed that the output voltage remained almost unchanged as long as the input-voltage transient is above the output voltage-hold threshold. The solution also avoided reverse current from occurring when the input voltage was lower than the output voltage-hold threshold. Additionally, a stringent and monotonous startup waveform was achieved when the input voltage recovered.

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