DC-DC Power Conversions and System Design Considerations for Battery Operated System

Lingyin Zhao and Jinrong Qian, Texas Instruments

ABSTRACT

The demand for portable devices such as cellular phones, PDAs, MP3 players and portable DVD players has grown significantly during the last few years. The portable devices usually include a variety of loads including LCD display, memories, mini microprocessor, Universal Series Bus (USB), and a hard disk drive. These loads require different operating voltages and load currents, and are powered by the rechargeable batteries such as Lithium-ion (Li-Ion) batteries, Nickel Metal Hydride (NiMH) batteries and Silver-Zinc batteries through DC-DC converters. Among them, the lithium-ion (Li-Ion) battery is widely-adopted because of its high energy density on both a gravimetric and volumetric basis. To achieve longer system run-time and smaller size, more and more system designers are focusing on improving a system's power conversion efficiency with advanced circuit topologies through a better understanding of the battery characteristics. This paper first reviews the typical Li-Ion battery discharge characteristics and then discusses five commonly used DC-DC converters in portable power devices. Light load efficiency improvement, output voltage regulation accuracy, battery impedance impact on the system efficiency and system stability are also analyzed in detail.

I. INTRODUCTION

While demands for portable power electronics have grown significantly during the last a few years, end users are more concerned about the battery run-time. Extending the battery run-time becomes the top priority for the system designers. This paper overviews five commonly used DC-DC conversion topologies suitable for battery operated systems: Buck, Boost, non-inverting Buck-Boost, Charge Pump and Flyback converters. The operation principle and basic operation characteristics of these converters are analyzed with the selection guide of various topologies according to different applications. Some design considerations associated with portable power design have been discussed, such as light load efficiency, voltage regulation accuracy, the battery impedance impact on the end of discharge voltage, battery discharge efficiency and system stability.

I. LI-ION BATTERY DISCHARGE CHARACTERISTICS

A portable device needs a battery as its power source when an AC adapter is not available. The battery plays a very important role in the system performance such as system run-time and system stability. Fig. 1 shows the Li-Ion battery discharge characteristics under different discharge rates. During the battery discharging period, the Li-Ion battery voltage discharges from 4.2 V at fully charged state to 3.0 V at the end of discharge voltage (EDV). The battery voltage reaches the EDV earlier under higher discharge current than under lower discharge current due to the battery internal impedance effect. This means that the useable battery capacity is smaller at the higher discharge rate than at the lower discharge rate. Thus, lower discharge rate is able to increase the useable capacity and extend the battery run-time when the battery is close to the deeply discharged state.

Fig. 2 shows battery discharge characteristics under different battery temperatures, specifically that the Li-Ion battery has less useable capacity with a high-discharge rate at lower temperature than at higher temperature due to high internal impedance at lower temperature. However, the battery is still able to deliver a reasonable capacity even below 0°C with a low discharge rate since the voltage drop across the battery internal impedance is not significant.

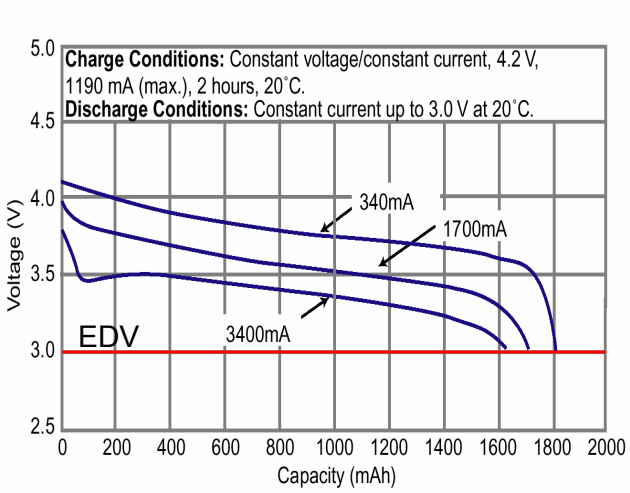

Fig. 1. Typical Li-ion battery discharge characteristics under different discharge rates.

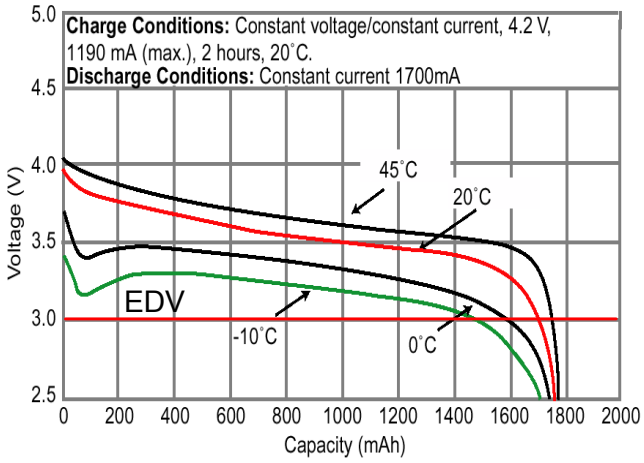

Fig. 2. Typical Li-ion battery discharge characteristics under different temperatures

The typical portable power system includes the mini-micro processor, display, memories, I/O interface, and hard disk, each of which requires a different operating voltage rail. Fig. 3 shows the typical range of battery voltages and system voltages.

These voltages are derived from the battery and are required DC-DC converters including the LDO, Buck, Boost, Buck-Boost, Flyback, and charge pump converters. Among them, the switching DC-DC converters are more efficient than LDO and charge pump converters, but more expensive and complicated.

Designing a high efficiency DC-DC converter for these portable devices is challenging due to the special requirements of a battery operated system, such as a wide input voltage variation and dynamic operating load. The following sections, present the fundamentals and design considerations of various portable DC-DC conversion topologies including Buck, Boost, non-inverting Buck-Boost, Flyback and Charge Pump converters.

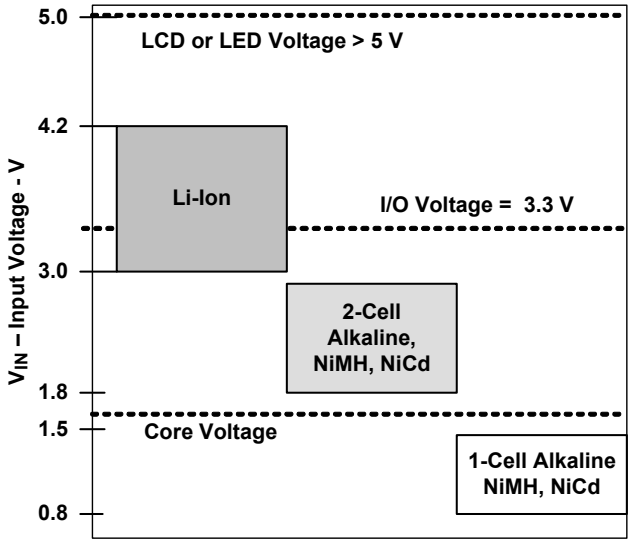

Fig. 3. Typical battery operating voltage range and system voltages.

III. DC-DC CONVERTER TOPOLOGIES

A. Buck Converter

The Buck converter is employed to achieve high efficiency and extend the battery run-time where a linear regulator cannot be used because of its high power dissipation for high-load current, or high input/output voltage difference applications. As a means of reducing the DC voltage and achieving voltage and current regulations, a Buck converter uses non-dissipative components, such as switches, inductors and capacitors. The non-synchronous topology is shown in Fig. 4(a).

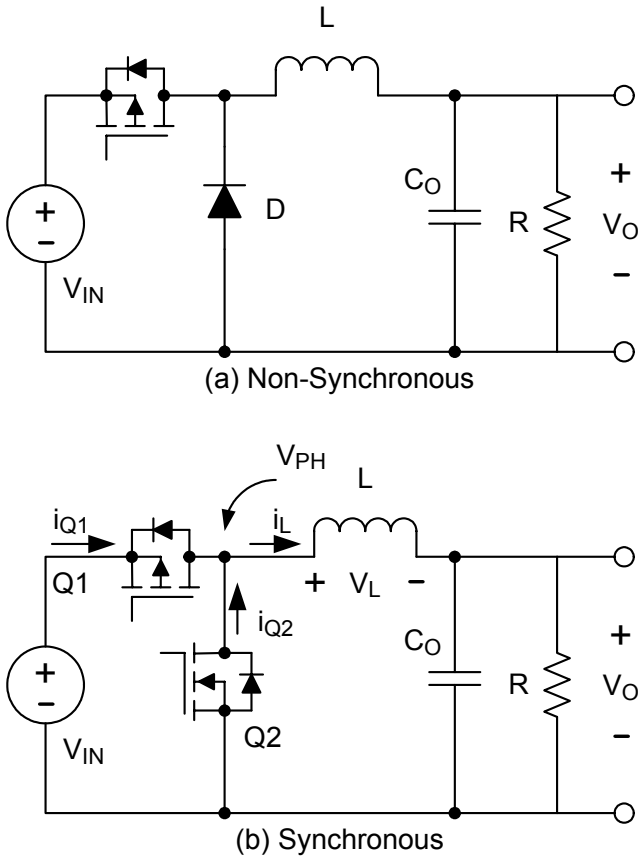

Fig. 4. Buck converter schematics.

For achieving higher efficiency for low-output voltage applications, the diode D is replaced with a MOSFET in a synchronous Buck converter[1] since the voltage drop across a MOSFET is lower than that of a Schottky diode (typically between 0.3 V and 0.5 V), resulting in higher power conversion efficiency and longer battery run-time. A synchronous Buck converter is shown in Fig 4(b). The two switches alternately turn on and off to regulate the output voltage in response to the input voltage variation and dynamic load transients.

The key waveforms of a synchronous buck converter in continuous conduction mode (CCM) are shown in Fig. 5. Prior to t_1, the body diode of Q2 is conducting. When Q1 is on at t_1, the voltage at the phase node V_{PH} is V_{IN}. The inductor current increases linearly. When it turns off at t_2, the inductor current flows through the body diode of Q2 and the voltage at V_{PH} falls to a diode drop below ground. The dead time from t_2 to t_3 is required to avoid the shoot through current between two switches Q1 and Q2. Q2 turns on at t_3 with an almost zero drain to source voltage resulting in lower turn-on switching loss.

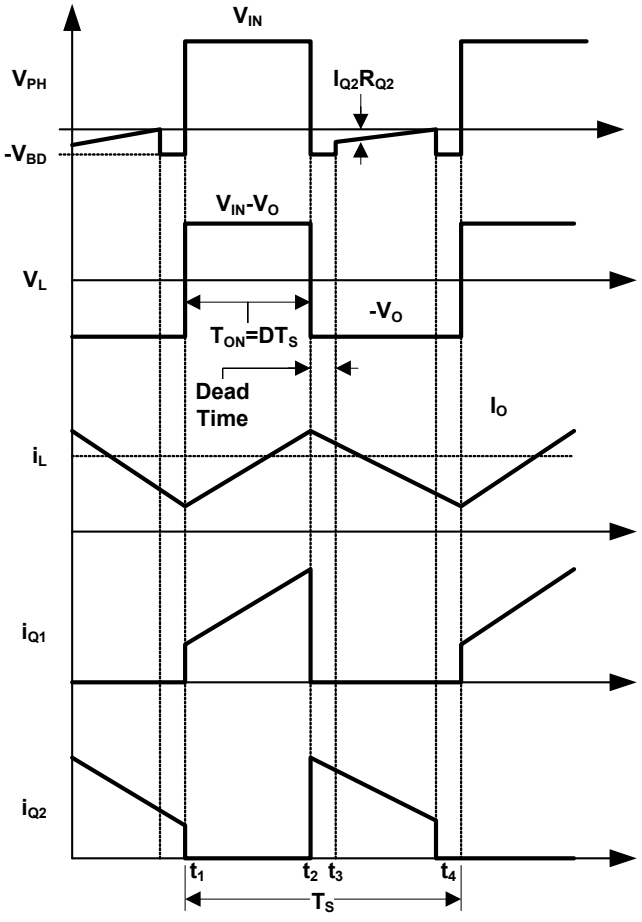

Fig. 5. Key waveforms of a synchronous buck converter in CCM.

The inductor current goes through Q_2 instead of its body diode. Q2 turns off at t_4 and the inductor current free wheels to the body diode of Q2. Therefore, Q2 turns off with almost zero voltage, resulting in lower turn-off switching loss. It is shown that the voltage at V_{PH} is rectangular ranging between V_{IN} and ground with a *high* time of T_{ON}. The L, C_O filter is added in series between V_{PH} and V_O and yields a clean, low-ripple DC voltage at V_O.

In steady state, the net volt-seconds applied to an inductor over one switching cycle must be zero, i.e. Equation (1).

$$(V_{IN} - V_O) \bullet DT_S = V_O(1-D)T_S \tag{1}$$

Solving for the voltage gain is described in Equation (2).

$$\frac{V_O}{V_{IN}} = D \tag{2}$$

Considering the on-resistance of the MOSFETs and DCR of the inductor, the required duty cycle is larger to compensate for the voltage drop across the switchers and inductor in order to regulate output voltage. Similarly, net voltage second across the inductor must be zero over a switching cycle.

$$\begin{aligned}&(V_{IN} - I_O R_{Q1} - I_O R_L - V_O) \bullet DT_S \\ &= \left(V_O + I_O R_{Q2} + I_O R_L\right)(T_S - DT_S)\end{aligned} \tag{3}$$

The voltage gain can be derived in Equation (4).

$$D = \frac{V_O + I_O\left(R_{Q2} + R_L\right)}{V_{IN} + I_O\left(R_{Q2} - R_{Q1}\right)} \tag{4}$$

where

- R_{Q1} is the on-resistance of MOSFET Q1
- R_{Q2} is the on-resistance of MOSFET Q2
- R_L is the DCR of the inductor
- R is load resistance

The voltage gain of an ideal synchronous Buck and a non-ideal synchronous Buck with various load resistances are shown in Fig. 6 assuming R_{Q1}=50 mΩ, R_{Q2}=50 mΩ and R_L=50 mΩ. Fig 6 shows it requires a higher duty cycle at a heavy load than at light load because it has the higher voltage drop across the MOSFETs and inductor, which requires higher duty cycle to compensate for this voltage drop.

If the Li-Ion battery is used as an input voltage source, it is very possible for the buck converter to operate in dropout mode when the battery voltage drops to near the output voltage. The converter can not regulate the output voltage even with maximum duty cycle of 1, where the switch Q1 is always on. The maximum available output voltage is given by Equation (5)

$$V_{O(\max)} = V_{IN} - I_O(R_{Q1} + R_L) \tag{5}$$

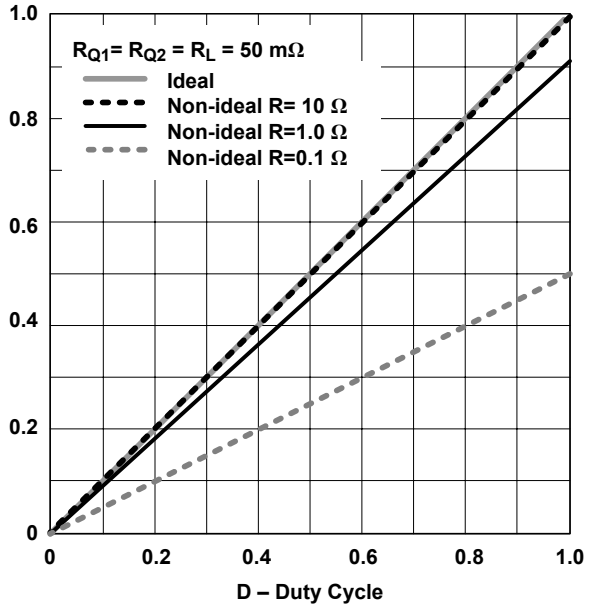

Fig. 6. Voltage gain of a Buck converter as a function of duty cycle.

The inductor ripple current can be obtained by using Equation (6).

$$\Delta I_L = \frac{V_{IN} - V_O}{L}\frac{V_O}{V_{IN}} \bullet \frac{1}{f_S} \tag{6}$$

The inductor is selected in such a way that the inductor ripple current ΔI_L is chosen to be a practical 30% of the load current. Assuming all inductor ripple current flows into the output capacitor, the voltage ripple due to limited output capacitance and its equivalent series resistance (ESR) is given by the following equations:

$$\Delta V_{O\_C_o} = \frac{V_O \bullet (1 - D)}{8LC_O \cdot f_S^{\,2}} \tag{6}$$

$$\Delta V_{O\_ESR} = \Delta I_L \bullet ESR \quad (7)$$

ΔV_{O_Co} has 90° phase delay with respect to the inductor current while ΔV_{O_ESR} is in phase with the inductor current. Thus, these two output ripple voltage components have 90° phase shift. The voltage ripple due the output capacitor is usually designed to be less than 1% of the output voltage.

B. Boost Converter

The Boost converter is another well-known switching mode converter that is capable of producing a DC output voltage greater in magnitude than the DC input voltage. Fig 7(a) shows the basic non-synchronous boost converter in portable power applications. Use a synchronous Boost converter[2] shown in Fig 7(b), where a MOSFET Q2 is used to replace the Schottky diode when the output voltage is not very high, for improving power conversion efficiency.

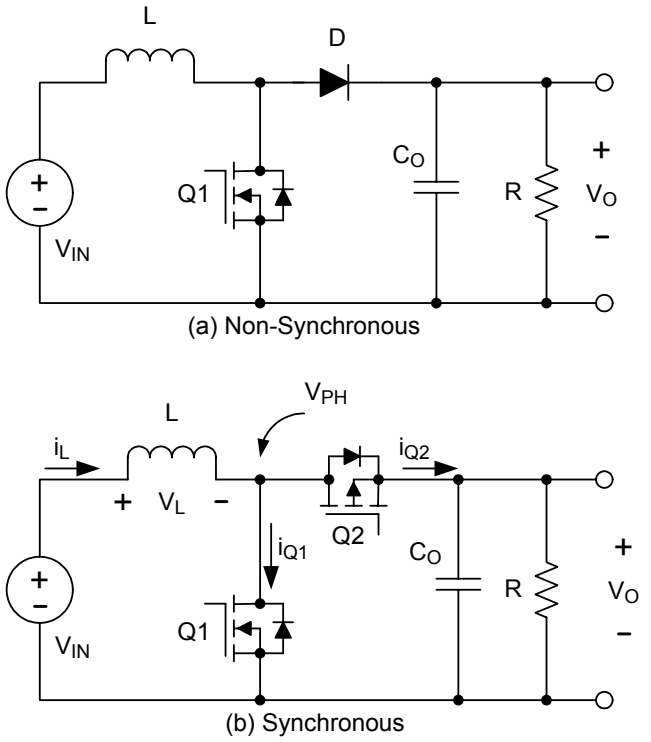

Fig. 7. Boost converter circuits.

The key waveforms of a synchronous Boost converter in CCM are shown in Fig. 8. Prior to Q1 conduction at t_1, the body diode of Q_2 is on. When Q_1 turns on at t_1, the input voltage V_{IN} is applied to the inductor and the inductor current linearly increases. At the same time, the output capacitor is discharged and supplies the load current. Q1 turns off at t_2 and the inductor current flows through the body diode of the MOSFET Q2. During the dead time period from t_2 to t_3, both MOSFETs Q1 and Q2 are off to prevent shoot through current from output to ground. The synchronous MOSFET Q2 turns on at t_3 with zero voltage (body diode voltage drop) resulting in less turn-on switching loss.

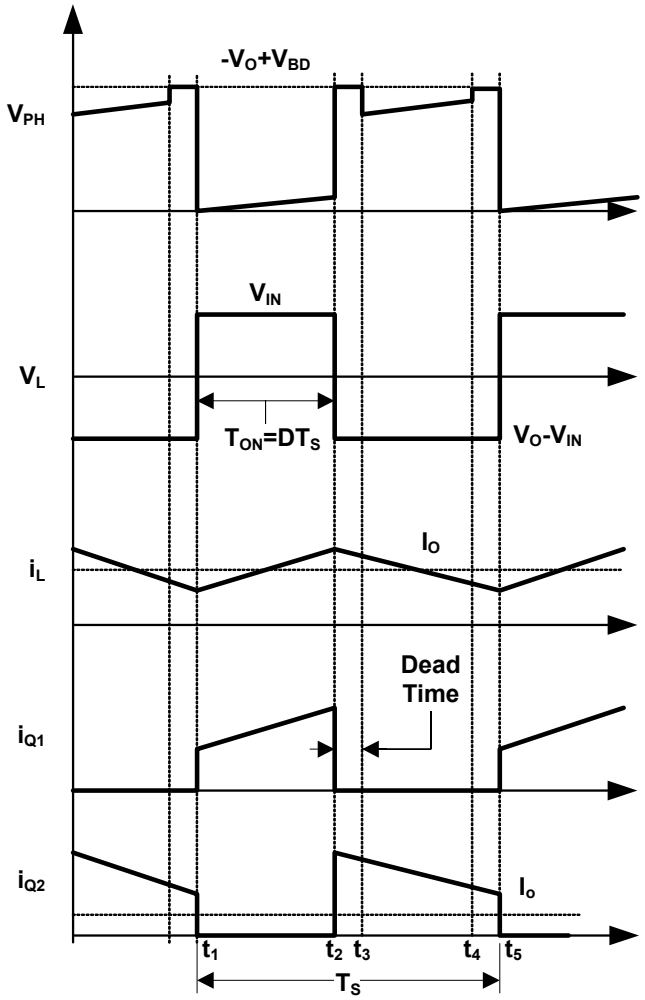

Fig. 8. Key waveforms of a Boost converter in CCM.

The inductor current flows through the MOSFET Q2 instead of its body diode to reduce the conduction loss and deliver power to the output. The synchronous MOSFET Q2 turns off at t_4 and the inductor current flows through its body diode. The MOSFET Q1 turns on again at t_5, and the body diode is reverse biased and turns off. The reverse recovery current through the body diode of Q2 flows through the MOSFET Q1, which causes a reverse recovery loss in Q1.

To derive the voltage gain, the voltage second across the inductor must be zero over a switching cycle under CCM in steady state. Assume there is no power loss across Q1, Q2 and inductor, applying voltage-second balance principle gives Equation (8).

$$V_{IN} \cdot D \bullet T_S = (V_O - V_{IN})(1-D) \bullet T_S \tag{8}$$

Solving for the voltage gain yields Equation (9).

$$\frac{V_O}{V_{IN}} = \frac{1}{1-D} \tag{9}$$

where

- D is the duty cycle of Q1

Considering the on-resistance of Q1 and Q2, and DCR of the inductor, voltage gain taking the resistive losses on the switches and the inductor into account is given by:

$$\frac{V_O}{V_{IN}} = \frac{1}{1-D} \bullet \frac{1}{1 + \dfrac{R_L + D \bullet R_{Q1} + (1-D) \bullet R_{Q2}}{(1-D)^2 \bullet R}} \tag{10}$$

The voltage gain of an ideal Boost and a non-ideal Boost with various load resistances are shown in Fig. 9, assuming R_{Q1}=50 mΩ, R_{Q2}=50 mΩ and R_L=50 mΩ.

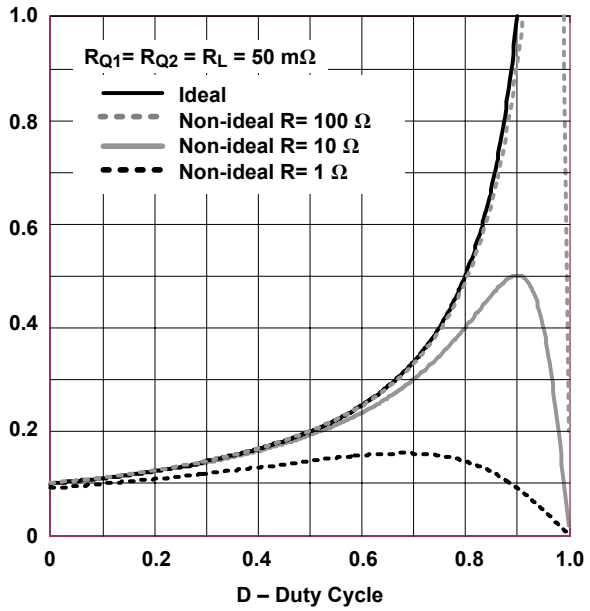

Fig. 9. Voltage gain of a synchronous Boost converter as a function of duty cycle.

It can be seen that the output load has a significant impact on the voltage gain. For the ideal boost converter without any power loss, when the duty cycle D approaches one, the voltage gain is infinity. However, the voltage gain curve tends to zero rather than approaching infinity at D=1 for the practical converter. This is because there is no time for a boost converter to deliver the energy stored in the inductor to the output if the switch Q1 is always on. It is difficult for an actual boost converter to achieve higher than voltage gain of 10. Therefore, Flyback (introduced in later section) is normally employed to achieve a very high output voltage.

The minimum output voltage is achieved with zero duty cycle, where Q1 is always off and Q2 is always on. This minimum output voltage is given by Equation (11).

$$V_{O(\min)} = V_{IN} - I_O(R_L + R_{Q2}) \tag{11}$$

However, it is very difficult for a boost converter to achieve the output voltage between $V_{O(min)}$ and V_{IN} since the required duty cycle for Q1 is too small to be properly controlled.

C. Non-inverting Buck-Boost Converter

Given a wide range of battery discharge voltage from 3.0 V to 4.2 V for a single cell Li-Ion battery, the required system operation voltage could be higher or lower than the battery voltage. This requires the DC-DC converter have buck-boost capability. Traditional buck-boost and Cuk converters are capable of achieving this function, but it provides a negative output voltage. Fig. 10(a) shows a non-inverting buck-boost converter[3]. It is essentially a cascade combination of a Buck converter followed by a Boost converter, where an inductor is shared by both Buck and boost converter[4]. For improving the system power conversion efficiency, a synchronous Buck-Boost converter is usually used in portable power applications, as shown in Fig 10(b).

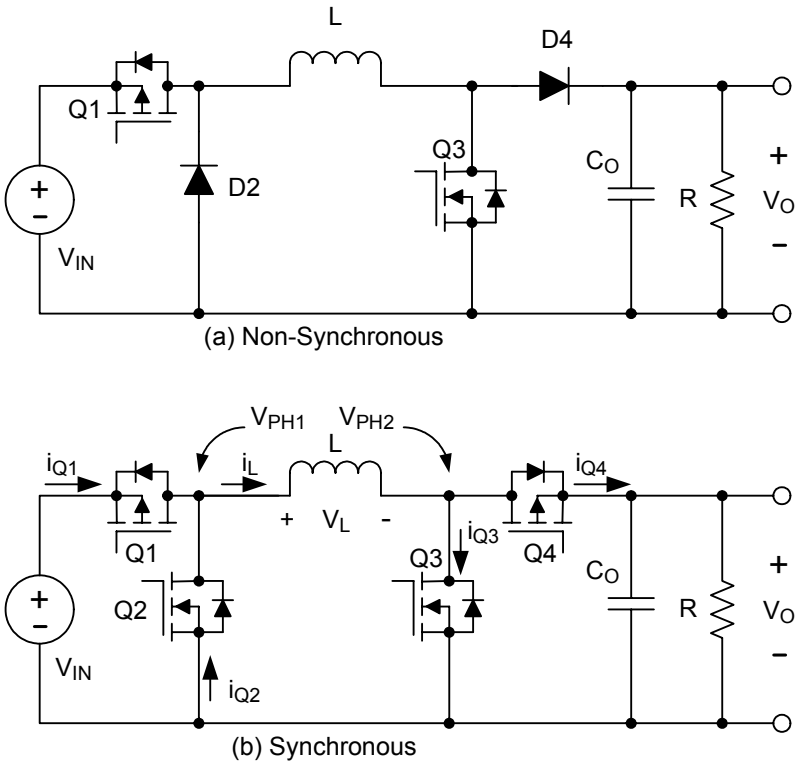

Fig. 10. Non-inverting Buck-Boost converter.

There are two control schemes to achieve Buck-Boost function for the circuits shown in Fig 10.

Control Scheme No. 1:

The key switching waveforms are presented in Fig. 11. When switches Q1 and Q3 simultaneously turn on at t_1, the input voltage is applied across the inductor. The inductor current increases linearly and the output capacitor provides power to the load. When Q1 and Q3 turn off at t2, the inductor current flows through both the body diodes of Q2 and Q4 until at t3. During the dead time interval from t2 to t3, all MOSFETs are off to prevent the shoot through between Q1 and Q2, and between Q3 and Q4. When Q2 and Q4 turn on at t_3 with a zero voltage (voltage drop across the body diode) resulting in lower turn-on switching loss across Q2 and Q4. During this time period, the inductor current flows through Q2 and Q4, and delivers its stored energy to the output. Both synchronous MOSFETs Q2 and Q4 turn off at t_4, and their body diodes turn on until both control MOSFETs Q1 and Q3 turn on at t_5.

Assuming no power loss across the switcher and inductor, the voltage gain with this control scheme under CCM is given by Equation (12).

$$\frac{V_O}{V_{IN}} = \frac{D}{1-D} \tag{12}$$

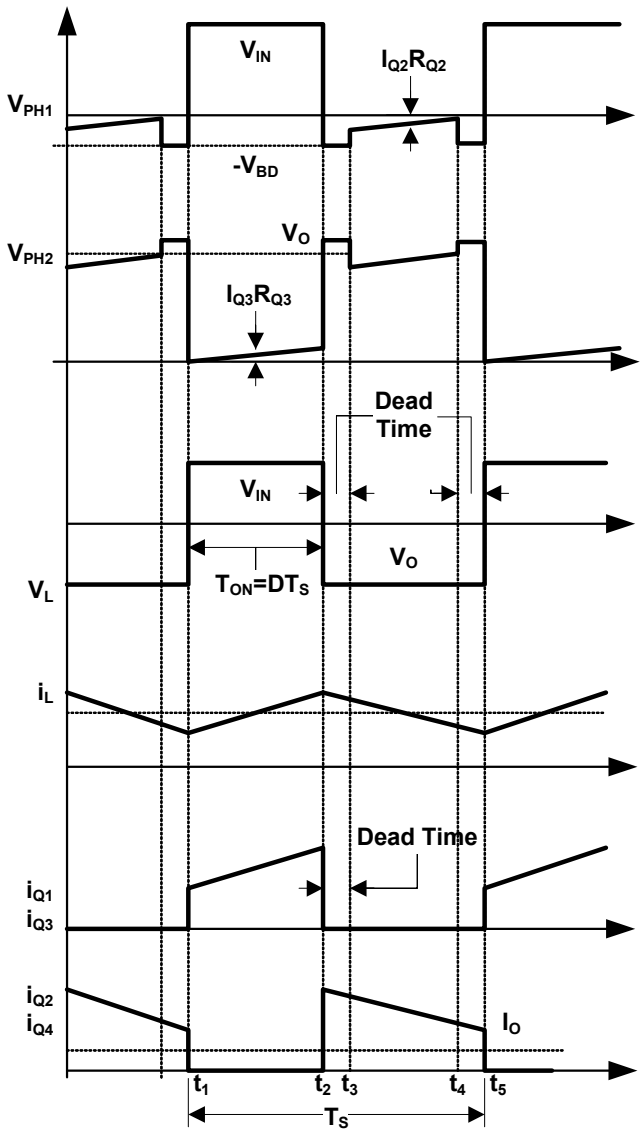

Fig. 11. Key waveforms of a non-inverting, synchronous Buck-Boost DC-DC converter.

For the duty cycle of 0.5, the output voltage is equal to the input voltage. The output voltage is lower than the input voltage for a duty cycle less than 0.5, and the output voltage is higher than the input for the duty cycle greater than 0.5. In order to achieve the same output voltage as the input voltage, the duty cycle of 0.5 is needed. Therefore, the Buck-Boost converter with this control scheme is more practical and easier than either Buck or Boost converters to achieve the voltage gain of 1.

Control Scheme No. 2:

The converter can operate in either the Buck mode or Boost mode. The operating mode depends on the input and output voltages.

Buck Operation Mode: When V_{IN} is above V_O, Q4 is always on while Q3 is always off. Q1 and Q2 turn on and off complimentarily as a synchronous Buck converter..

Boost Operation Mode: When V_{IN} is below V_O, Q1 is always on while Q2 is always off. Q3 and Q4 turn on and off complimentarily as a synchronous Boost converter.

Both Buck and Boost converters have difficulty achieving the same output voltage as the input voltage. The buck converter can achieve the maximum output voltage of V_{IN}-I_O(R_{Q1}+R_{Q4}+R_L) only with 100% duty cycle while the Boost converter can achieve minimum output voltage of V_{IN}-I_O (R_{Q1}+R_{Q4}+R_L) with 0% duty cycle. It looks like that there is an ideal smooth voltage transition between Buck converter and Boost converter.

However, it is really difficulty for a Boost converter to regulate the output voltage a little higher than V_{IN}-I_O(R_{Q1}+R_{Q4}+R_L) due to very small duty cycle operation, which is limited by the minimum on-time of the MOSFETs. Therefore, the mode transition from Buck operation mode to Boost operation mode or vice versa may not be smooth. Pay attention to this transition and properly design the control loop to achieve smooth transition. The advantage of the Control Scheme No. 1 is that the operation mode transition is very smooth around duty cycle of 0.5.

With Control Scheme No. 1, each of the input and output pairs of transistors are activated as diagonal pairs in every cycle. Turning on the Q1 and Q3 switching pair enables the inductor to store the energy from the input power source, while turning on the Q2 and Q4 switching pair makes the inductor deliver its energy to the output and charge the output capacitor. Note that in each mode, two switches turn on and off at the same time. Therefore the switching losses of the Classic 4-Switch converter is doubled than those of a Buck or Boost converter.

When the input voltage equals the output voltage, where D is equal to 0.5, the inductor current is given by two times of the load current. Because the inductor current is twice the load current, the conduction losses are four times that of a Buck or low duty cycle Boost converter. The physical size of the inductor must also be larger to accommodate this extra current without saturation. Also, it has higher switching losses since the switchers have to turn on and off with higher switching current. Apparently, the Control Scheme No. 2 has an improved efficiency because only two switches are in operation during any clock cycle. As the time that the converter connects the input to the output via the inductor is maximized. This further improves the efficiency compared with the Control Scheme No. 1.

D. Flyback Converter

The flyback converter is actually an isolated traditional Buck-Boost converter. It employs a transformer to isolate between the input and output as depicted in Fig. 12. Both Boost converter and Buck-Boost converter have inherent voltage gain limitation due to the on-resistance of the MOSFETs and DCR of the inductor. However, the Flyback converter has one more parameter, transformer turns ratio, to achieve high voltage gain. Since the Flyback converter has minimum number of external components compared with other isolated topologies, it is suitable for high voltage and low power applications[5]. The synchronous flyback converter is not as popular as other synchronous switching converters because the current through the output diode is relatively small with high output voltage and the voltage drop across the diode D is very small compared with the output voltage. Because of that, the synchronous flyback converter will not be discussed here.

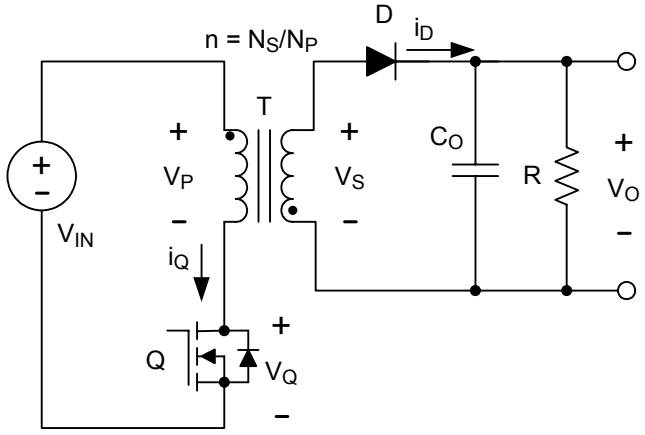

Fig. 12. Flyback converter.

In CCM mode with the ideal switcher, the voltage-second balance across either of the transformer windings must be zero over one switching cycle in steady state. This yields Equation (13).

$$V_{IN} \bullet D \cdot T_S = \frac{V_O}{n}(1-D) \bullet T_S \tag{13}$$

Solving the voltage gain leads to

$$\frac{V_O}{V_{IN}} = n \bullet \frac{D}{1-D} \tag{14}$$

where

- n is the transformer turns ratio of secondary winding to the primary winding.

So the voltage gain of the Flyback converter is similar to that of the buck-boost converter, but with a factor of n. The key waveforms of a Flyback converter are shown in Fig. 13.

The flyback converter is commonly used for low-power and high-voltage applications, for example, the photoflash circuit for digital camera application. It has the advantage of very low parts count. Multiple outputs can be obtained by using a minimum number of parts and each additional output requires only an additional winding, diode, and a capacitor with cross regulation.

The peak MOSFET voltage is equal to $V_{IN}+ V_O/n$, as shown in Fig 13.

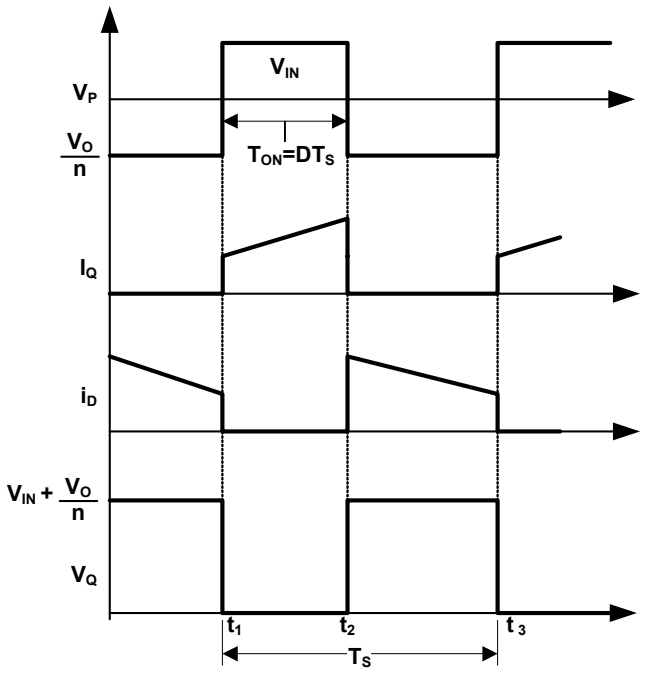

Fig. 13. Key waveforms of a Flyback converter in CCM.

In practice, additional voltage spike is observed due to ringing associated with the transformer leakage inductance and output capacitance of the switch Q and winding parasitic capacitance. An R-C-D snubber circuit is usually required to clamp the magnitude of this ringing voltage to a safe level so that a low voltage rating device can be used as shown in Fig 14.

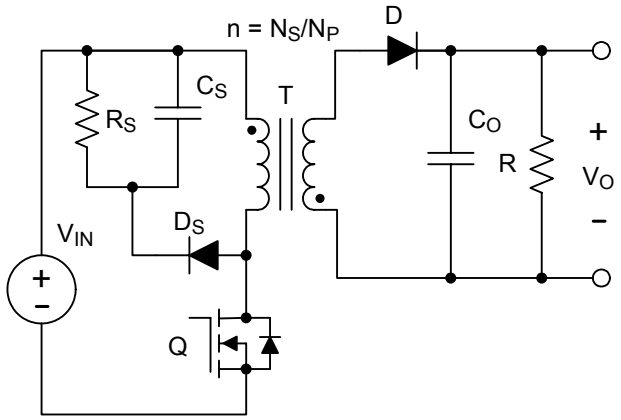

Fig. 14. Flyback converter with R-C-D snubber.

E. Charge Pump Converter

Charge pump circuits are well known as voltage doublers or inverters for very low power applications, e.g. below 200 mA of output current[6]. A charge pump circuit usually provides a voltage that is higher than the voltage of the input power supply. Switching converters use inductors as energy storage devices while charge pump circuits use capacitors as energy storage devices. The basic configuration for a charge pump converter is shown in Fig. 15.

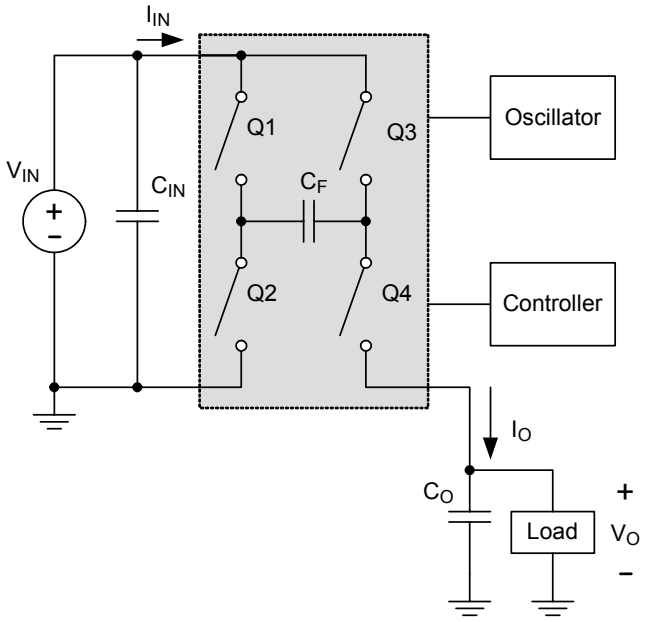

Fig 15. Basic charge pump circuit.

The operation of a charge pump converter can be divided into two phases: In Phase 1, also called charge phase, the switches Q2 and Q3 are closed and the flying capacitor C_F is ideally charged to V_{IN}. During this time period, the output capacitor C_O supplies the load and is therefore being discharged. At the end of Phase 1, Q2 and Q3 are turned off. In Phase 2, also called transfer phase, the switches Q1 and Q4 are closed and the flying capacitor C_F is placed in series to the input voltage. These two voltage sources charge the output capacitor C_O and supply the load. Phases 1 and 2 have a duty cycle of 50%. To transfer energy from the input to the output, the phases are periodically repeated with a frequency of several hundred kHz. A control circuitry and an oscillator control the operation of the charge pump.

The output voltage ripple depends on the time duration of the charge phase, the capacitor size and it's ESR.

In a dual low ripple charge pump converter, the two single-ended charge pumps operate with 180° out of phase, as shown Fig 16. The oscillator signal has a 50% duty cycle. Each single-ended charge pump transfers charge into its transfer capacitor (C_{F1} or C_{F2}) in one-half of the period. During the other half of the period (transfer phase), C_{F1} or C_{F2} is placed in series with the input to transfer its charge to C_O. While one single-ended charge pump is in the charge phase, the other one is in the transfer phase. This operation ensures an almost constant output current which ensures a low output ripple.

There are two possible regulation schemes: pulse-skip regulation and constant-frequency regulation. In pulse-skip regulation, the output voltage is held constant by skipping unneeded pulses. As long as the output voltage is below the required value, the charge pump operates and charges the output capacitor. If the output voltage exceeds a certain internally set level, the charge pump stops operation.

The constant frequency regulation system regulates the output voltage by adjusting the on-resistance of switches (MOSFETs). The charge pump operates all the time independent of the output voltage.

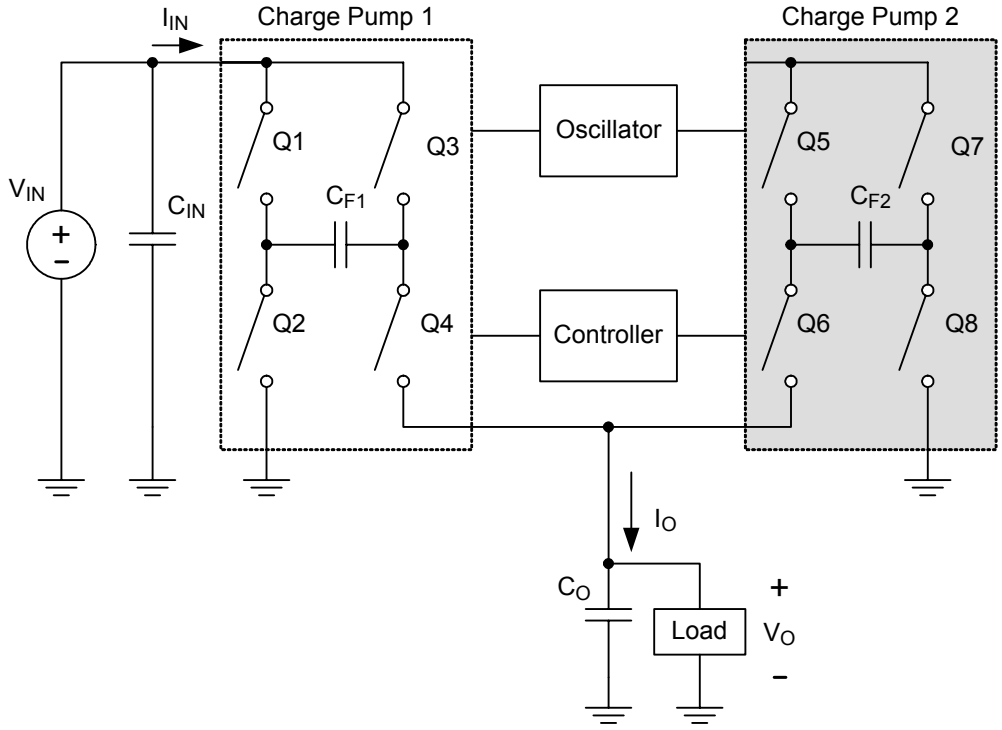

Fig 16. Dual low ripple charge pump converter.

The advantage of pulse-skip regulation is a very low quiescent current, because the charge pump operates only if the output voltage is below the regulation point. The disadvantages are the variable frequency and the higher output voltage ripple compared to constant frequency regulation.

The typical efficiency curves of a charge pump converter with pulse-skip and constant frequency regulation are shown in Fig 17. The charge pump converter can also achieve efficiency higher than 90%, depending on the input and output voltages, and charge pump gain. It can be seen that the converter achieves the highest efficiency when $V_O = 2V_{IN}$. The higher the input voltage, the lower the efficiency due to the higher voltage drop on the switching devices. The drawback of a charge pump converter is the limited gain, and low efficiency when the input and output voltage does not match the charge pump gain.

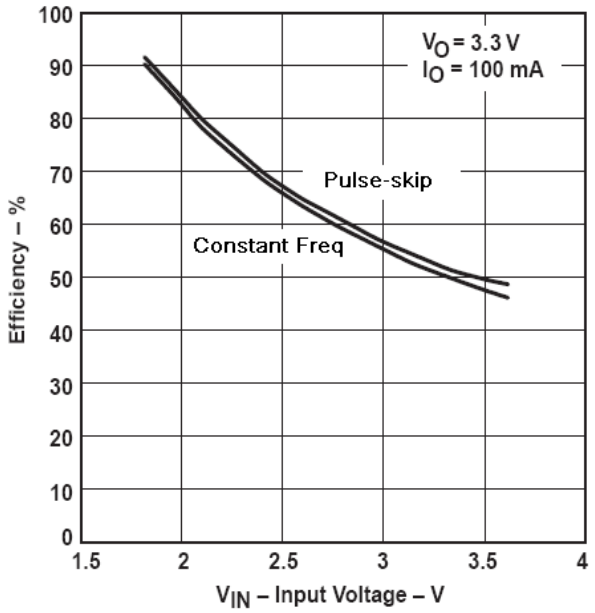

Fig. 17. Typical efficiency curves of a charge pump converter.

IV. Battery Operated System Design Considerations

A. Topology Selection

The topology selection is the first step of a portable power circuit design. It is mainly based on the input and output voltage rating, as shown in Fig. 18. If the input voltage is higher than the output at any time, a Buck converter or LDO is normally the only solution. If the input voltage is lower than the output voltage, a Boost converter can be employed while a charge pump converter could be used for low current and low cost applications. Both Buck-Boost and Flyback can be used for the case that the battery voltage can be either higher or lower than the output voltage. However, Flyback is normally more suitable for a higher output voltage case.

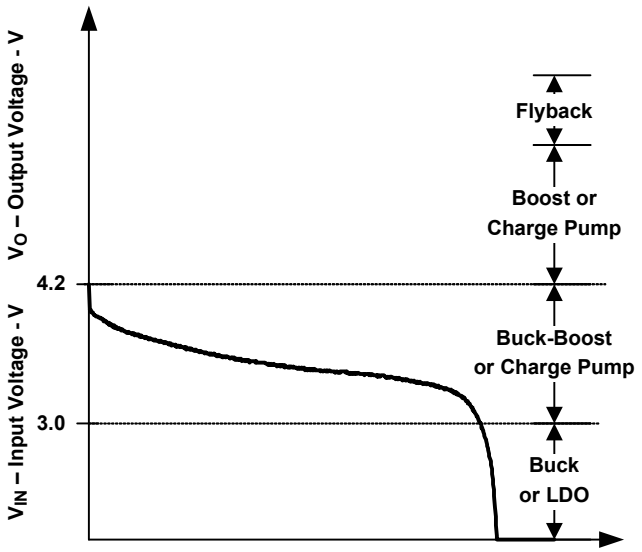

Fig. 18. Voltage considerations for topology selection for single-cell Li-ion battery applications.

B. General Guide for Selecting Battery Configuration

The battery selection is based on the battery cost, size, capacity, system power and voltage requirements. The Li-Ion battery has highest volumetric and gravimetric power density. Single cell Li-Ion battery has operating voltage range from 3.0V to 4.2 V or 4.4V depending on the battery chemistry, which is able to power majority system loads through high efficiency switching regulators. It is ideal for space limited applications such as mobile phone. However, it has highest cost. On the other hand, Alkaline, NiMH and NiCd batteries have lower cost than Li-Ion battery, but they usually have lower volumetric and gravimetric power density than L-Ion battery. The operating voltage range for these batteries is usually between 0.9 V and 1.35 V, which needs a boost converter to power the majority system loads. It should be noted that the high voltage gain boost converter has lower power conversion efficiency. Therefore, it usually needs two battery cells in series instead of in parallel in order to achieve high power conversion efficiency for the DC-DC regulators. See the information detailed battery selection based on structure, capacity and safety.[7].

C. Light Load Efficiency

Taking a synchronous Buck converter as an example, it operates in synchronous, continuous conduction mode when the load current is higher than the half inductor ripple current. The inductor current flows in the positive direction toward the output during an entire switching cycle, constantly supplying current to the load. In this mode, the synchronous switch is on whenever control switch is off, so the current always flows through a low impedance switch channel, minimizing voltage drop and conduction loss. This is the most efficient operation mode, where the conduction losses in the power devices are usually dominant. The ripple current depends on inductor value, switching frequency and output voltage, but is constant regardless of load as long as the converter remains in constant frequency operation. Forced continuous operation maintains a constant frequency throughout the entire load range, making it easier to filter the switching noise and reduce RF interference which is important for EMI-sensitive applications.

As the output load current decreases in continuous mode, the average inductor current reaches a point where it drops below half the ripple current. At this point, the current in the inductor reverses during a portion of the switching cycle, or begin to flow from the output back to the input as shown Fig. 19.(a).

This operation does not adversely affect regulation, but does cause additional conduction loss as a portion of the inductor current flows back and forth through the power switches, lowering the efficiency.

There are some benefits to allowing this reverse current flow.

- output voltage maintains regulation even if the inductor current drops below zero
- output ripple voltage and frequency remain constant at all loads, easing filtering the output ripple components

In addition to the additional loss associated with the inductor circulating current, the MOSFET gate drivers are still switching on and off once a cycle. Each time a MOSFET is turned on and off, the driver must charge and discharge its gate charge.

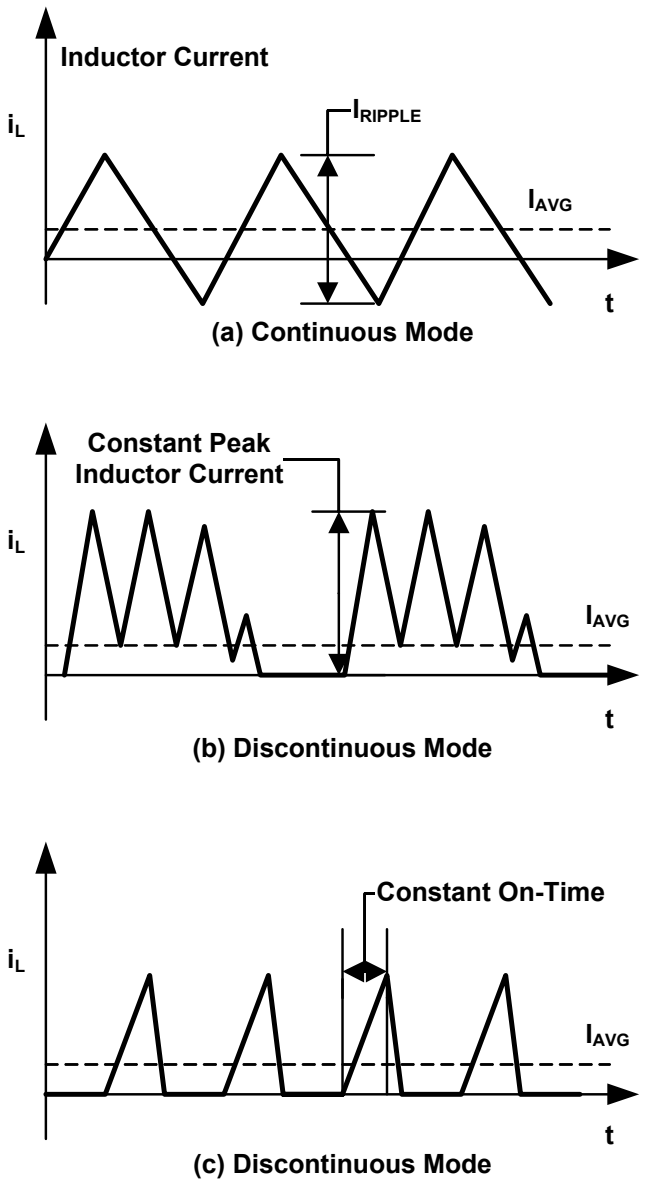

Fig. 19. Inductor current waveforms.

The gate driver losses are proportional to the switching frequency. As the load current continues to drop, this quickly becomes the dominant power loss, reducing efficiency further.

Today's power supply IC's for portable battery powered systems need to be optimized for highest power conversion efficiency over a very wide load current range. This allows the system manufacturer to build more powerful and complex systems while maintaining long battery standby time. The power supply system should operate at high efficiency at the nominal load current.

Some systems have to operate in a standby mode where the load current is reduced to a few milliamperes or even down to the microampere range when no backup batteries for RAM and real time clock are used. Even under these light load current conditions the power supply should be able to operate with a high efficiency. The load for the portable devices is highly dynamic with a wide range of load variation. It draws high current in active mode such as in talking mode for cellular phone applications and very low current in standby mode for most of the time.

At higher load currents the conduction losses of the MOSFETs are the dominant factor in determining the overall efficiency, whereas at light load, the switching losses and the static losses become more dominant. As a result, they reduce the efficiency at light load quite dramatically. Minimizing the static and switching losses at light load would increase the efficiency.

The static losses are mainly caused by the quiescent current of the converter device and other circuit leakage currents. The lower the quiescent current, the higher the efficiency at light loads. This can be achieved by designing the IC for very low quiescent currents where most of the circuitry is in shut down mode as the load current approaches zero.

The TPS62000, for example, has a typical quiescent current of just 50 μA. If external feedback resistors are used to program the desired output voltage, they need to be of high impedance in the MΩ range, depending on the output voltage. The switching losses are mainly caused by the high side and low side MOSFETs turning on and off. One way to reduce these losses is to reduce the switching frequency as the load current decreases. This can be achieved by using a PFM scheme, which requires converter operate in discontinuous conduction mode (DCM) with a low frequency operation at light load. The inductor current in DCM is shown in Fig. 19(b) and Fig. 19(c), depending on the control method.

In DCM operation, the PWM controller detects when the inductor current approaches zero and it turns off the low-side MOSFET. This eliminates the conduction loss associated with this inductor circulating current. In order to regulate the output voltage, the converter is able to reduce switching frequency by using constant peak current turn-off as shown in Fig. 19(b) or by using constant on-time control. This effectively reduces the switching frequency and minimizes the switching loss and gate drive loss to further improve the light load efficiency. The constant on-time control architecture has smooth mode transition from DCM to CCM or vice versa since it can inherently and continuously adjust the off-time to regulate the output voltage.

D. Voltage Regulation Accuracy

Output voltage regulation accuracy is one of the key specifications for any DC-DC converter. The output voltage accuracy mainly depends on internal reference voltage accuracy, feedback voltage accuracy, internal error amplifier DC gain and its offset voltage, feedback resistor divider accuracy, and system voltage loop DC gain. The feedback voltage at the non-inverting input of the voltage error amplifier specifies the possible voltage tolerance associated with the internal band-gap voltage reference through a voltage buffer over the full temperature range. This usually includes the offset voltage of the internal voltage error amplifier. It should be noted that the lower the feedback voltage, the higher the contribution tolerance due to the offset voltage.

The closed loop DC gain has a significant impact on the DC regulation accuracy. The higher the DC gain of the voltage loop, the higher the output voltage regulation accuracy. This is why a low-frequency pole such as an integrator is usually placed in the voltage loop compensator. The output voltage error ΔV_O in the closed voltage loop is given by Equation (15).

$$\frac{\Delta V_O}{V_{REF}} = \frac{1}{1 + G_1 G_2 G_3} \qquad (15)$$

where

- V_{REF}, is the voltages at the non-inverting error amplifier
- G_1 is the DC gain of the voltage error amplifier with loop compensator
- G_2 is the PWM comparator gain
- G_3 is the power stage gain from duty cycle to output voltage

The DC gain of the error amplifier also plays a very important role in the DC regulation accuracy, which usually is not specified in the PWM controller IC. If the converter has an overall closed loop DC voltage gain of 40 dB, i.e. $|G_1 G_2 G_3| = 40\,dB$, then the output has 1% tolerance due to the limited DC loop gain. In addition, the output feedback resistor divider is the other major contributor to DC error. Using 1% accuracy resistors adds 1% to the total output error budget.

E. Battery Impedance Effect on System Performance

Battery impedance plays a very critical role in the battery operated system. It affects the overall system efficiency, battery run-time and useable battery capacity. Fig. 20 shows the single cell Li-Ion battery impedance as a function of state of charge (SOC) and temperature. The Li-Ion battery has much higher impedance when deeply discharged than when fully charged. It has almost 3 to 4 times higher impedance at SOC=5% than at SOC=100% under the same battery temperature. In addition, the battery impedance exponentially increases when the temperature decreases. Thus, the battery dissipates more power under low temperature and a deeply discharged state because of its high internal impedance.

The battery discharge efficiency depends on the equivalent load connected into the battery pack terminals, which is given by Equation (16).

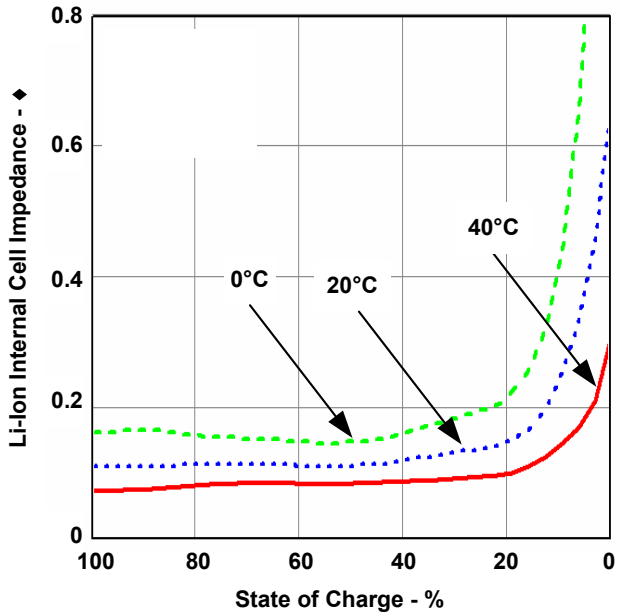

Fig. 20. Li-Ion battery impedance characteristics.

$$\eta = \frac{R_L}{R_{BAT} + R_L} \times 100 \quad (\%) \qquad (16)$$

Where R_L and R_{BAT} are the equivalent load connected to the battery terminals and battery DC impedance, respectively. Fig. 21 shows the battery discharge efficiency with a constant 3-Ω load connected to the battery terminals.

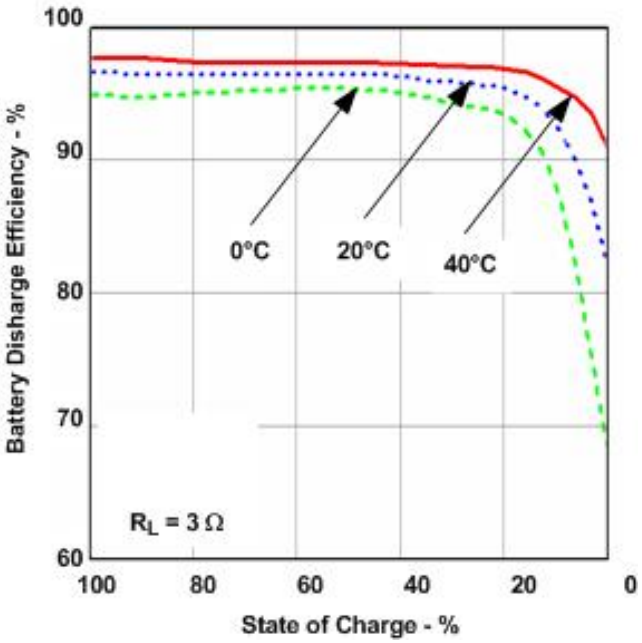

Fig. 21. Battery discharge efficiency.

It is shown that the battery has higher than 95% discharge efficiency with SOC greater than 20% and has as low as 70% discharge efficiency at the end of discharge. The battery itself dissipates about 30% energy when it approaches the end of discharge at 0°C. One way to efficiently deliver the battery energy to the load when the battery reaches the deeply discharged state is to reduce the system load so that the energy dissipated by the battery internal impedance can be minimized and improve the battery discharge efficiency.

For the system with fixed EDV, it reaches EDV faster at high system load and low temperature than at low system load and high temperature because of high voltage drop across the battery impedance. This results in useable battery capacity loss and shorter battery run-time. In order to improve the useable capacity and battery run-time, once the battery runs into the deeply discharged state by detecting the battery voltage, we can reduce the system load such as by dimming a bright display or even turning off the display, slowing down the speed of the hard disk drive, and throttling the microprocessor clock frequency.

It is also desirable for the host to provide power management in such a way that it avoids any high loads operating simultaneously to avoid high peak current. So, it is possible for the battery to operate from discharge curve A to discharge curve B to increase the useable battery capacity up to 15% as shown in Fig. 22.

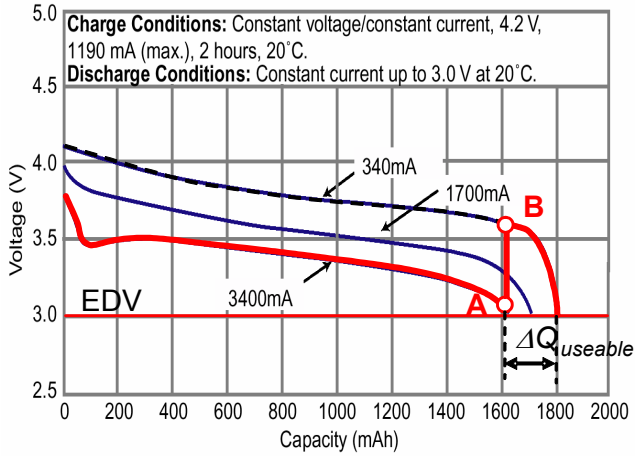

Fig. 22. Battery operation discharge curves

Another recommendation is to add enough decoupling capacitance to the high speed loads to eliminate the high slew rate current and avoid occasional early shutdown due to high spike battery discharge current.

The battery internal impedance may also impact the system stability in both steady state and during dynamic transients. The battery pack and the DC-DC converter actually form a cascaded system. The output impedance of the battery is Z_{OUT} and the input impedance of the DC-DC converter is Z_{IN}, as depicted in Fig. 23. V_{BAT} is the open-circuit battery voltage. The battery impedance Z_{BAT} includes DC resistance and AC resistance.

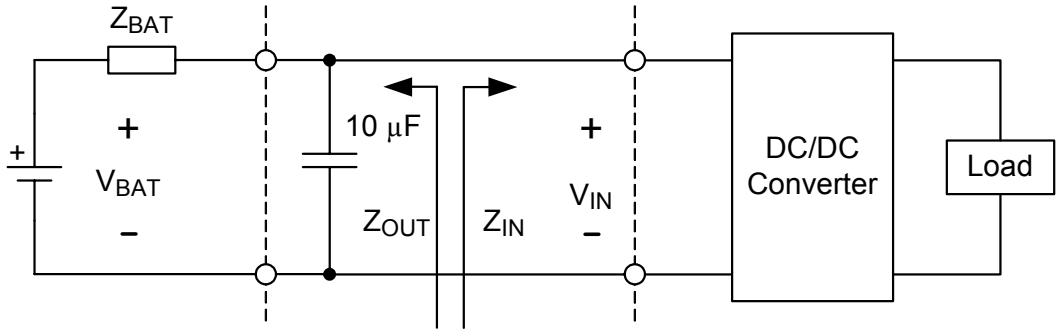

Fig 23. Impedances at the interface of two subsystems.

The solid curve in Fig. 24. shows the DC-DC converter I-V curve with a constant output power. The dashed line is the resistor load line with $-1/R_{BAT}$ slope for the battery under DC operating condition, where R_{BAT} is the DC battery impedance. To avoid bi-stability in the system, the load line should not intersect the DC-DC converter curve at or below V_{MIN}/I_{MAX} at any operating conditions.

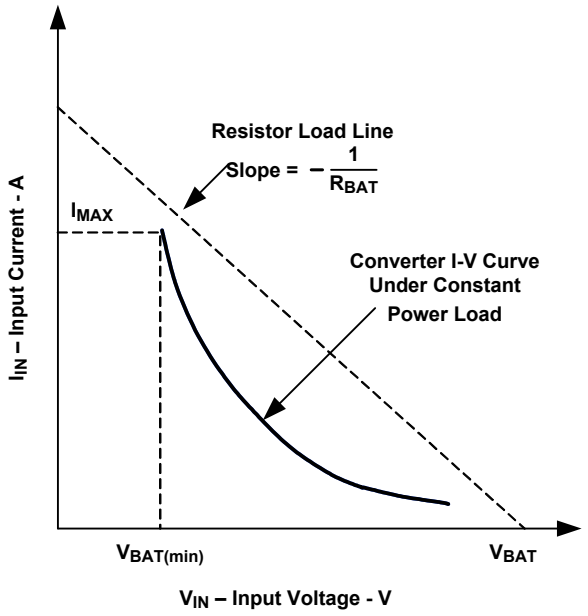

Fig. 24. Converter current/voltage curve and resistor load line

Fig. 25 shows the typical Li-Ion battery equivalent circuit model used to the following AC stability analysis. lt is approximately correct for charged state from 100% of SOC to 20% of SOC. Impedance varies from manufacturer to manufacturer up to two times and from cell to cell up to ±15%. For a discharged state below 20% of SOC the impedance starts to increase very rapidly. The particular value the impedance reaches depends on manufacturer, but it can be roughly modeled by multiplying R1 and R2 by 3.

As demonstrated in [8], the stability of a cascaded system can be analyzed using impedances at the interface of two subsystems. If both of the subsystems are stable, the sufficient condition for the stability of the entire system is $Z_{OUT} < Z_{IN}$ for all frequencies. The typical small-signal impedance Z_{OUT} of a Li-ion battery is shown in Fig. 26, where a 10-µF ceramic capacitor with 10-mΩ ESR and 10-nH ESL is in parallel with the battery pack. The Z_{IN} of a Buck converter input impedance with a closed loop leads to stability when these two curves are intersected. If there is an overlap between the output impedance of the battery pack and input impedance of a DC-DC converter, there is a system interaction between two cascade systems may result in unstable system. One possible solution to prevent such instability is to insert a filter either a capacitor or inductor and capacitor combination between two subsystems to separate the battery impedance from the input impedance of a DC-DC converter.

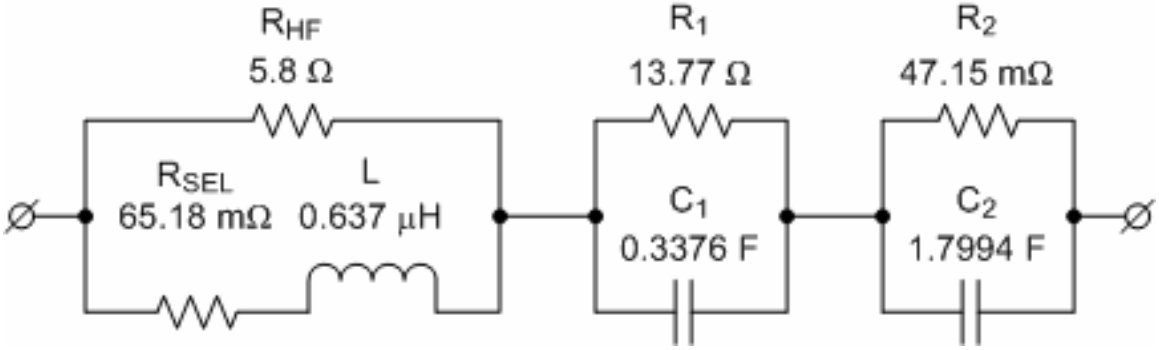

Fig. 25. Single cell Li-Ion battery equivalent circuit model (18560)

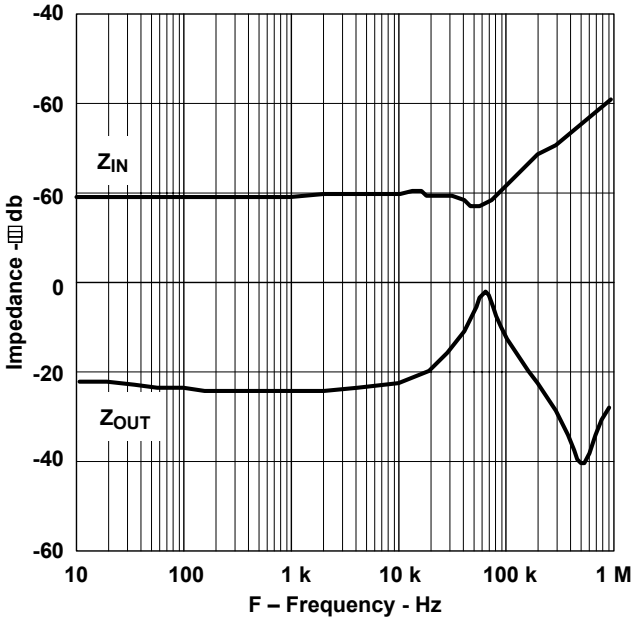

Fig. 26. Output impedance of a Li-ion battery and the input impedance of a Buck converter.

V. CONCLUSION

This paper reviews the typical battery discharge characteristics under different discharge rates and temperatures. The following five commonly used DC-DC topologies were reviewed for battery operated system: Buck, Boost, non-inverting Buck-Boost, charge pump and Flyback converters. Output voltage regulation accuracy, light load efficiency, system design considerations to improve the battery run-time, and battery impedance impact on the system stability were analyzed in detail. Fully understanding the battery characteristics help in designing the system to avoid early unexpected shutdown and improve the useable capacity and battery run-time.

VI. ACKNOWLEDGEMENT

Authors would like to thanks Oliver Nachbaur, Jürgen Neuhäusler, Bruce Hunter, Charles Mauney and Dave Freeman for their valuable suggestions and discussion.

VII. REFERENCES

[1] TPS62000 Datasheet, 600-mA 1-MHz High-Efficiency Step Down Low Power DC-DC Converter.

[2] TPS6101x Datasheet, High-Efficiency 1 cell and 2 cell Boost Converter.

[3] B. Sahu and G. A. Rincón-Mora, *A low voltage, dynamic, non-inverting, synchronous buck-boost converter for portable applications*," IEEE Trans. on Power Electronics, vol. 19, No. 2, pp. 443-452, March 2004.

[4] R. W. Erickson and D. Maksimović, Fundamentals of Power Electronics, 2nd ed., Kluwer Academic Publishers, Sixth Printing 2004.

[5] TPS65552A Datasheet, Integrated Photo Flash Charger and IGBT Driver.

[6] B. Kormann, *High-efficiency, Regulated Charge Pumps For High-Current Applications*, 2001 Unitrode Design Seminar, 2001.

[7] Yevgen Barsukov, TI portable power seminar 2005, *Battery Selection, Safety And Monitoring In Mobile Applications*.

[8] B. H. Cho, B. Choi, *Analysis And Design Of Multi-Stage Distributed Power Systems*" The 13th International Telecomunications Energy Conference, pp. 220 – 226, 5-8 Nov. 1991.